REMARKS

By this Amendment, claims 5 and 15 are amended and claim 21 is added. Accordingly, claims 1-5, 5-13 and 15-21 are pending in this application. Reconsideration of the application is respectfully solicited.

Applicants gratefully acknowledge the courtesies extended to Applicants' representative at the personal interview conducted on March 1, 2004. The substance of the interview is incorporated in the following remarks, which constitute Applicants' record of the interview.

The Office Action objects to claims 5 and 15 for informalities. By this Amendment, the informalities are corrected, thereby obviating the objection. Applicants respectfully request that the objection be withdrawn.

The Office Action rejects claims 1-3, 5-13 and 15-20 under 35 U.S.C. §103(a) over U.S. Patent No. 5,301,325 to Benson in view of U.S. Patent No. 5,261,062 to Sato. This rejection is respectfully traversed.

The Office Action admits that Benson does not teach that the controller "divides the source code into code blocks based on a target processor register capability, wherein the controller identifies source register types as data registers or address registers of the source processor and corresponding target registers of the target processor that correspond to each of the source register types, the controller selecting one or more selected source register types and one or more maximum numbers of corresponding target registers that correspond to the selected source register types as the target register capability," as recited in both independent claims 1 and 11. The Office Action relies on Sato to allegedly provide the missing subject matter.

However, Applicants submit that Sato discloses a system which translates a program written in a high order language for programming to output a sequence of machine-oriented

words adapted for pipelining. (Column 1, lines 11-14). "Pipelining" is defined in col. 1, lines 44-53, as "pipeline control is performed to increase processing speed. The pipeline control provides control whereby one instruction is divided into a plurality of steps, and during execution of some step of the instruction, some step of another instruction is executed. According to this control, it is possible to execute a plurality of instructions during a unit period of time which formerly permitted only one instruction to be executed, and thus to increase processing speed as the whole." Sato further discloses in col. 2, lines 50-54, that "it is therefore an object of the present invention to provide a register allocation system adaptive for pipelining capable of improving the optimizing of instruction relocation adaptive for pipelining, and thus reducing disturbance of the pipe."

Thus, Sato is concerned only with providing a register allocation system for a single processor, which improves the performance of the processor when operating under pipeline control. For example, in col. 4, lines 63-69, Sato discloses "Fig. 3 is a flowchart which allows an operation of the system by a central processing unit (CPU) 14, Fig. 9, according to the present invention" (emphasis added). Therefore, the system described in Sato is disclosed as having only one processor CPU 14. Consequently, there are no "source processor" and "target processor," as the program is translated to run on the same processor CPU 14.

During the personal interview, the Examiners asserted that the source processor is inherent because Sato discloses translating code from a source program. Applicants respectfully disagree.

Sato discloses only translating a source program to a machine-language program, by compiling the source program into an intermediate format program comprising pseudo-codes. The pseudo-codes are virtual machine oriented instructions which are not limited in the number of registers used (see column 1, lines 19-27). A virtual register, used to store the

operand of a pseudo-code instruction, is identified in the Office Action as corresponding to the source registers.

However, the virtual registers do not imply that a source processor exists. The virtual registers are a tool or construct for assisting in the translation of a high-level source program into a low-level, machine-language program, each program being executable on the same processor. Therefore, there is no source processor disclosed in Sato, as distinct from the target processor, because Sato is not concerned with translating code as run on one processor to code to run on another processor.

Therefore, Applicants submit that disclosing a source program does not inherently disclose a source processor, because as set forth above, the source program may run on the same processor as the translated target code, and in fact, in Sato, it does. As repeatedly set forth in Federal Circuit decisions, an anticipatory inherent feature or result must be consistent, necessary, and inevitable, not merely a possibility or probability. For example, as set forth in Transclean Corp. v. Bridgewood Services, Inc., 290 F.3d 1364, 1373, 62 USPQ2d 1865 (Fed. Cir. 2002), "anticipation by inherent disclosure is appropriate only when the reference discloses prior art that must necessarily include the unstated limitation" (emphasis added).

Therefore, Sato does not disclose expressly or inherently that "the controller identifies source register types as data registers or address registers of the source processor," because no source processor is disclosed, taught or suggested in Sato.

Claims 2-3 and 5-10 depend from claim 1, and claims 12-13 and 15-20 depend from claim 11. Therefore, claims 2-3 and 5-10 are patentable for at least the reasons set forth above with respect to claim 1, as well as for the additional features they recite. Additionally, claims 12-13 and 15-20 are patentable for at least the reasons set forth above with respect to claim 11, as well as for the additional features they recite. Accordingly, Applicants

respectfully request that the rejection of claims 1-3, 5-13 and 15-20 under 35 U.S.C. §103(a) be withdrawn.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-3, 5-13 and 15-21 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Jaquelin K. Spong
Registration No. 52,241

JAO:JKS/aaw

Date: March 12, 2004

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461